ADC Board 4 Channel Notes

September 29, 2006 - **DRAFT - May not be correct**

Board Features

4 Chan - 130MSPS 16 bit ADCs LTC2208 - Data clocked into 64k Sample FIFOs

1 buffered clock input to CPLD
1 buffered trigger input to CPLD
2 unbuffered coax I/O from CPLD
3 digital I/O from CPLD
4 interrupts to uCdimm5282

Ethernet Port RJ45 connector
2nd Ethernet port using SMSC LAN9118 Ethernet Controller
1 COM Port to 9 pin D connector
1 COM Port to header
I2C Port to header
QSPI 4 wire Serial port with 4 chip selects to header
12 bit General Purpose I/O to header
6 10bit mux analog in or 4 digital I/O and 2 digital Outs to header

Various Info

Can't use chip selects 0, 3, 4, 5 and 6. CS0 boot select? CS3 not brought out? CS4, 5, and 6 are address lines. Only CS 1 and 2 can be used.
CS1, A2 and A3 run through the CPLD, we can use the CPLD to clock X words before the data we want.

IPSBAR default = 0x4000_0000

Slow analog in and Slow analog out will be done through the QSPI port

Timing

1k word at 119MHz = 8.6uS
1k word at 102MHz = 10.0uS

Read and move data takes time

Required number of samples for each system.

- S-Band Accelerator = 850nS = 88 samples
- X-accelerator = 100nS = 12 samples
- RF Gun = 64 samples
- T-cav = 100nS = 8 samples
- Phase Cavity = 1.25uS = 128 samples
- BPMs = ????

LTC2208 Board Notes

LTC2208 Functions

LVDS (Pin 61): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3V_{DD} selects demultiplexed CMOS mode. Connecting LVDS to 2/3V_{DD} selects Low Power LVDS mode. Connecting LVDS to V_{DD} selects Standard LVDS mode. - **GND**

MODE (Pin 62): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3V_{DD} selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3V_{DD} selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer. - **VDD - Resistor Selectable**

RAND (Pin 63): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference. - **- CPLD selectable**

PGA (Pin 64): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of 2.25V_{P-P}. High selects a front-end gain of 1.5, input range of 1.5V_{P-P}. **3.5dB difference - CPLD selectable**

SHDN (Pin 19): Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state. **20mS recovery time - CPLD selectable**

DITH (Pin 20): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation. **- CPLD selectable**

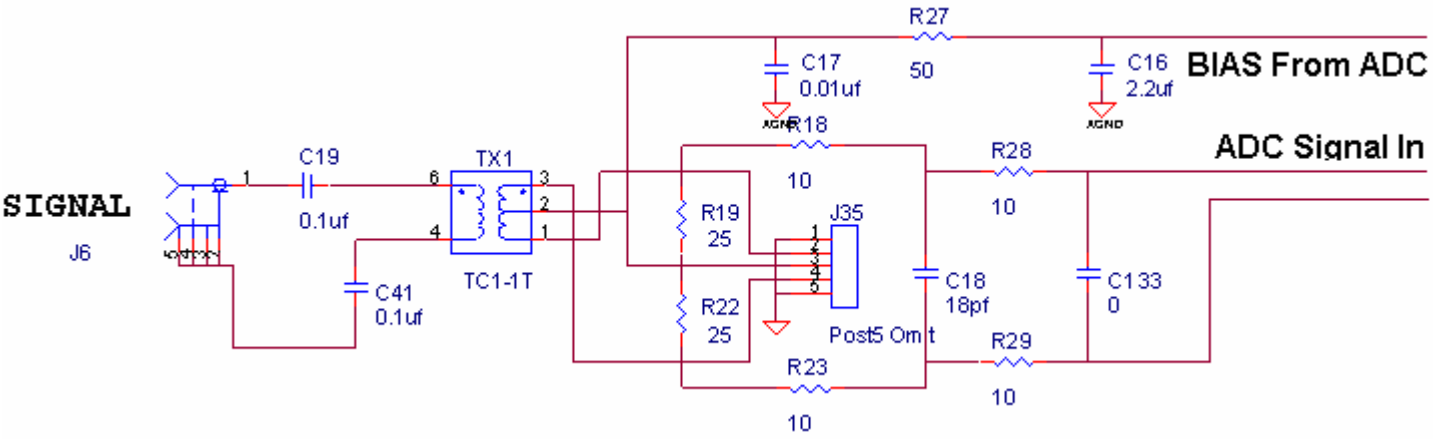
FIFO

FIFO OW (output width = 9, /18) pin 73 **GND**
FIFO /BE (not Big-Endian) pin 69 **GND**
FIFO /LD (Load-/PAE and /PAF Flags) **GND**
FIFO FWFT/SI (/Standard Mode) **GND**
FIFO FSEL0 FSEL1 (Flag value select) **GND**
FIFO IP (Interspersed Parity) **GND**
FIFO PFM (Prog Flag Mode) **GND**
FIFO RM (Retransmit Mode) **GND**
FIFO /RT (Retransmit) **VCC**
FIFO /SEN (Serial Enable) **VCC**
FIFO /WEN (Write Enable) - **CPLD** **Timing critical**
/WEN to /WCLK Tens=2.5nS Tenh=0.5nS
CPLD will resync trigger to write clock
FIFO /REN (Read Enable) - **CPLD separate 4 FIFOs**

FIFO /PRS - (Partial Reset) - **CPLD**
FIFO /MRS - (Master Reset) - **CPLD**
The FIFO needs time after reset pulse before writing.
/PRS should be used instead of /MRS
15nS Prior to /MRS or /PRS: **/REN, /WEN**, /RT, and /SEN must be high and stay high until after recovery.
Reset PW = 10nS and recovery is 10nS
FIFO /OE and RCLK for each FIFO are connected to the CPLD

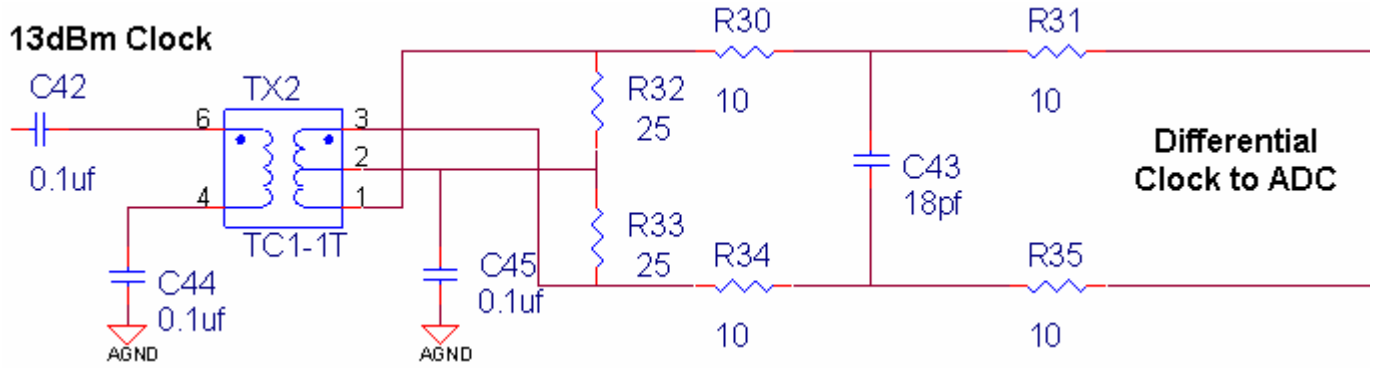
/FF (FiFO Full) - **Connect to TP**
/FE (FIFO Empty) - **Connect to TP**

Signal Input



The input signal for the ADC uses a Minicircuits transformer to level shift the inputs to the ADC bias. The 20ohm, 18pf, input filter attenuates sample and hold transients coming out of the ADC and bandwidth limits the input. The TC1-1T limits the input frequency from 400kHz to 500MHz. The ADC is set to run at 2.25Vpp, and the series resistors likely raise this another 5% depending on frequency.

Clock Input



The clock is input to the board at 21dBm and split 6 ways. Each of the 6 signals are about 13dBm. Four of the signals drive the ADC with the above circuit. One of the clocks drive the CPLD, and the other clock is routed to an SMA connector for off board use. The clock rate of the ADC is specified to be between 1MHz and 130MHz. The board has been tested at 102MHz.

Surface Mount

RF Transformer

TC1-1T

50Ω 0.4 to 500 MHz

CASE STYLE: AT224
PRICE: $1.19 ea. QTY (100)

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
RF Power	0.25W
DC Current	30mA

Pin Connections

PRIMARY DOT	6
PRIMARY	4
SECONDARY DOT	1
SECONDARY	3
SECONDARY CT	2
NOT USED	5

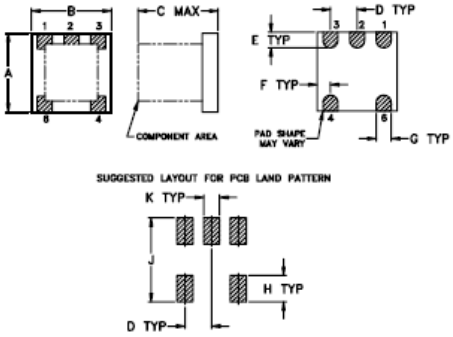
Features

- usable over 0.4-500 MHz
- excellent amplitude unbalance, 0.1 dB typ. and phase unbalance, 2 deg typ. in 1 dB bandwidth
- leadless surface mount
- good return loss
- aqueous washable

Applications

- VHF/UHF receivers/transmitters
- push-pull amplifiers

Outline Drawing AT224



Transformer Electrical Specifications

Ω RATIO	FREQUENCY (MHz)	INSERTION LOSS*			PHASE UNBALANCE (Deg.) Typ.		AMPLITUDE UNBALANCE (dB) Typ.	
		3 dB MHz	2 dB MHz	1 dB MHz	1 dB bandwidth	2 dB bandwidth	1 dB bandwidth	2 dB bandwidth
1	0.4-500	0.4-500	0.5-300	1-100	2	5	0.1	0.6

* Insertion Loss is referenced to mid-band loss, 0.35 dB typ.

Outline Dimensions (inch / mm)

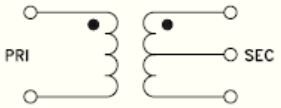
A	B	C	D	E	F
.150	.150	.150	.050	.030	.025
3.81	3.81	3.81	1.27	0.76	0.64

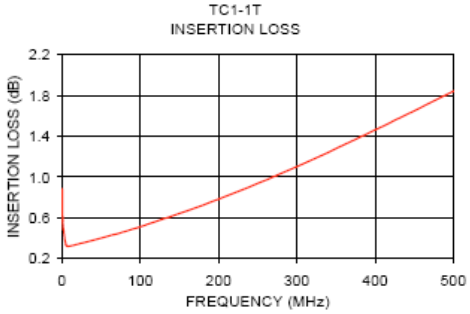
G	H	J	K	wt
.028	.065	.190	.030	grams
0.71	1.65	4.83	0.76	0.10

Typical Performance Data

FREQUENCY (MHz)	INSERTION LOSS (dB)	INPUT R. LOSS (dB)	AMPLITUDE UNBALANCE (dB)	PHASE UNBALANCE (Deg.)
0.30	0.88	15.46	0.06	0.03
1.00	0.57	21.01	0.04	0.05
5.00	0.33	27.35	0.02	0.01
10.00	0.32	28.55	0.02	0.15
50.00	0.40	23.46	0.02	0.63
100.00	0.51	18.34	0.06	1.24
200.00	0.78	13.01	0.21	2.57
300.00	1.10	10.06	0.47	3.99
400.00	1.46	8.16	0.82	5.66
500.00	1.84	6.90	1.26	7.50

Config. A





PARTS

Serial

SLAS449A–FEBRUARY 2005–REVISED MARCH 2005

16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converters

FEATURES

- **16-Bit Resolution**
- **2.7V to 5.5V Single-Supply Operation**
- **Very Low Power: 15µW for 3V Power**
- **High Accuracy, INL: 1LSB**
- **Low Glitch: 8nV-s**
- **Low Noise: 10nV/√Hz**
- **Fast Settling: 1.0µS**
- **Fast SPI Interface, up to 50MHz**
- **Reset to Zero-Code**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- **Industry-Standard Pin Configuration**

APPLICATIONS

- **Portable Equipment**
- **Automatic Test Equipment**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Optical Networking**

DESCRIPTION

The DAC8830 and DAC8831 are single, 16-bit, serial-input, voltage-output digital-to-analog converters (DACs) operating from a single 3V to 5V power supply. These converters provide excellent linearity (1LSB INL), low glitch, low noise, and fast settling (1.0µS to 1/2 LSB of full-scale output) over the specified temperature range of –40°C to +85°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

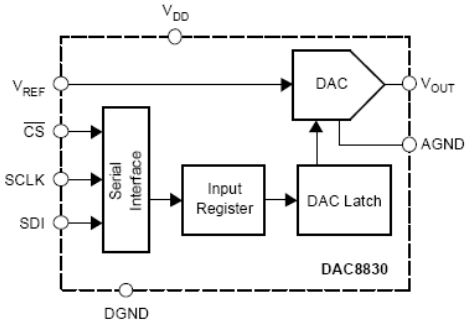
These parts feature a standard high-speed (clock up to 50MHz), 3V or 5V SPI serial interface to communicate with the DSP or microprocessors.

The DAC8830 output is 0V to V_{REF}. However, the DAC8831 provides bipolar output ($\pm V_{REF}$) when working with an external buffer. The DAC8830 and DAC8831 are both reset to zero-code after power up.

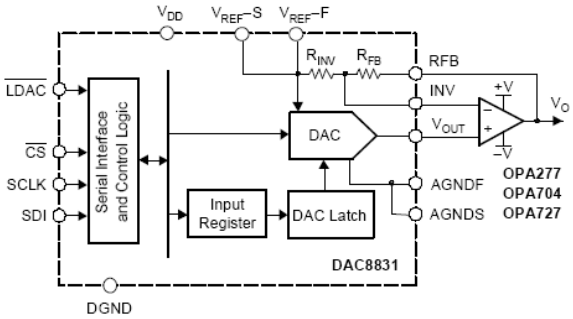
For optimum performance, a set of Kelvin connections to external reference and analog ground input are provided on the DAC8831.

The DAC8830 is available in an SO-8 package and the DAC8831 in an SO-14 package. Both have industry standard pinouts (see Table 3, the Cross Reference table in the *Application Information* section for details).

DAC8830
Functional Block Diagram



DAC8831
Functional Block Diagram



TI DAC8831

8-Channel, 24-Bit
ANALOG-TO-DIGITAL CONVERTER with FLASH Memory

FEATURES

- **24 BITS NO MISSING CODES**
- **0.0015% INL**
- **22 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)**
- **4K BYTES OF FLASH MEMORY PROGRAMMABLE FROM 2.7V TO 5.25V**
- **PGA FROM 1 TO 128**
- **SINGLE CYCLE SETTLING MODE**
- **PROGRAMMABLE DATA OUTPUT RATES UP TO 1kHz**
- **PRECISION ON-CHIP 1.25V/2.5V REFERENCE: ACCURACY: 0.2% DRIFT: 5ppm/°C**
- **EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 2.5V**
- **ON-CHIP CALIBRATION**
- **PIN-COMPATIBLE WITH ADS1216**
- **SPI™ COMPATIBLE**
- **2.7V TO 5.25V**
- **< 1mW POWER CONSUMPTION**

APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
- **LIQUID/GAS CHROMATOGRAPHY**
- **BLOOD ANALYSIS**
- **SMART TRANSMITTERS**
- **PORTABLE INSTRUMENTATION**
- **WEIGHT SCALES**
- **PRESSURE TRANSDUCERS**

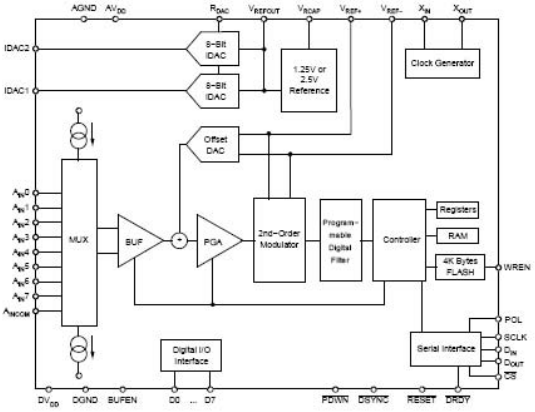
DESCRIPTION

The ADS1218 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution and Flash memory operating from 2.7V to 5.25V supplies. The delta-sigma, A/D converter provides up to 24 bits of no missing code performance and effective resolution of 22 bits.

The eight input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burnout current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog (D/A) converter provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable sinc filter. The reference input is differential and can be used for ratiometric conversion. The on-board current DACs (Digital-to-Analog Converters) operate independently with the maximum current set by an external resistor.

The serial interface is SPI-compatible. Eight bits of digital I/O are also provided that can be used for input or output. The ADS1218 is designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



TI ADS1218

Burr-Brown Products
from Texas Instruments

ADS8345

SBAS177C – FEBRUARY 2001 – REVISED APRIL 2003

16-Bit, 8-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- BIPOLAR INPUT RANGE
- PIN-FOR-PIN COMPATIBLE WITH THE ADS7844 AND ADS8344
- SINGLE SUPPLY: 2.7V to 5V
- 8-CHANNEL SINGLE-ENDED OR 4-CHANNEL DIFFERENTIAL INPUT
- UP TO 100kHz CONVERSION RATE
- 85dB SINAD
- SERIAL INTERFACE
- QSOP-20 AND SSOP-20 PACKAGES

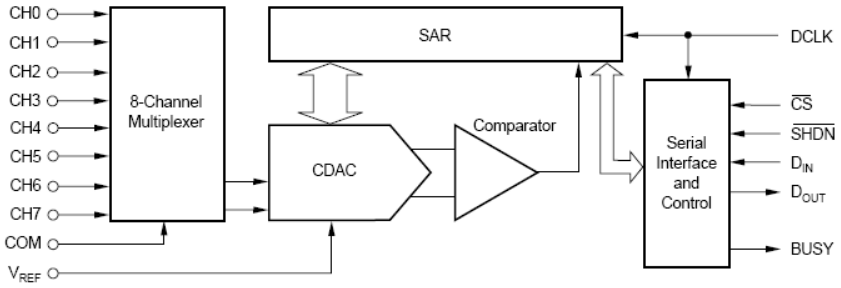
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS8345 is an 8-channel, 16-bit, sampling Analog-to-Digital (A/D) converter with a synchronous serial interface. Typical power dissipation is 8mW at a 100kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 500mV and $V_{CC}/2$, providing a corresponding input voltage range of $\pm V_{REF}$. The device includes a shutdown mode which reduces power dissipation to under 15µW. The ADS8345 is ensured down to 2.7V operation.

Low-power, high-speed, and an onboard multiplexer make the ADS8345 ideal for battery-operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS8345 is available in a QSOP-20 or SSOP-20 package and is ensured over the –40°C to +85°C temperature range.



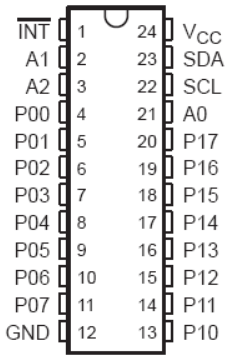
TI ADS8345

PCF8575
REMOTE 16-BIT I²C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT

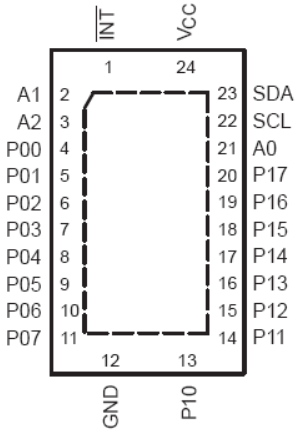
SCPS121B – JANUARY 2005 – REVISED SEPTEMBER 2005

- Low Standby-Current Consumption of 10 μA Maximum
- I²C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- 400-kHz Fast I²C Bus
- Address by Three Hardware Address Pins for Use of Up To Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Current Source to V_{CC} for Actively Driving a High at the Output
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

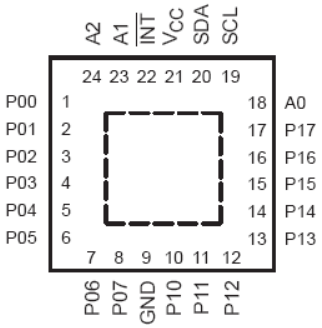
DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RHL PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)

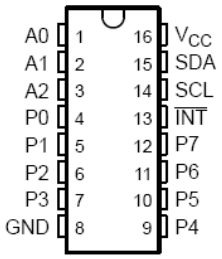


TI PCF8575

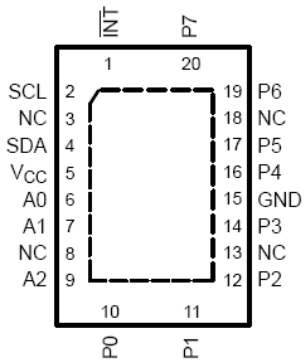
FEATURES

- **Low Standby-Current Consumption of 10 μA Max**
- **I²C to Parallel-Port Expander**
- **Open-Drain Interrupt Output**
- **Compatible With Most Microcontrollers**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DW OR N PACKAGE (TOP VIEW)

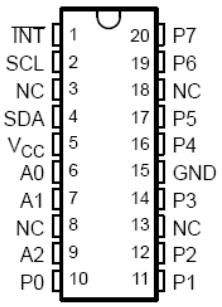


RGY PACKAGE (TOP VIEW)



NC – No internal connection

DGV OR PW PACKAGE (TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I²C) is designed for 2.5-V to 6-V V_{CC} operation.

The PCF8574 provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V_{CC} is active. An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

TI PCF8574